LISTING OF THE CLAIMS

1. (Original) A lookup table (LUT) in a field programmable gate array (FPGA), comprising:

a plurality of LUT input terminals;

a LUT output terminal;

a plurality of configuration memory cells, each memory cell having an output terminal; and

a plurality of CMOS pass gates coupled between the output terminals of the memory cells and the LUT output terminal, wherein each path between one of the memory cells and the LUT output terminal traverses at least two of the CMOS pass gates, the two CMOS pass gates being coupled to two different ones of the LUT input terminals.

2. (Original) The lookup table of Claim 1, wherein each path between one of the memory cells and the LUT output terminal traverses four of the CMOS pass gates.

3. (Original) The lookup table of Claim 2, wherein the four CMOS pass gates traversed by each path are coupled to four different ones of the LUT input terminals.

4. (Original) The lookup table of Claim 2, wherein the plurality of memory cells comprises 16 memory cells.

5. (Original) The lookup table of Claim 1, the plurality of CMOS pass gates including an additional CMOS pass gate on the path between each memory cell and the LUT output terminal, the lookup table further comprising:

a plurality of additional LUT input terminals; and

a decoder circuit having input terminals coupled to the additional LUT input terminals and output terminals coupled to gate terminals of the additional CMOS pass gates.

6. (Original) The lookup table of Claim 5, wherein the plurality of LUT input terminals comprises two input terminals and the plurality of additional LUT input terminals comprises two input terminals.

7. (Original) The lookup table of Claim 6, wherein the plurality of memory cells comprises 16 memory cells.

8. (Original) The lookup table of Claim 5, wherein the decoder circuit comprises:

a plurality of inverters having input terminals coupled to the plurality of additional LUT input terminals and further having output terminals; and

a plurality of NAND gates having input terminals coupled to the plurality of additional LUT input terminals and to the output terminals of the plurality of inverters and further having output terminals coupled to gate terminals of the additional CMOS pass gates.

9. (Original) The lookup table of Claim 1, further comprising a first inverter having an input terminal coupled to the LUT output terminal.

10. (Original) The lookup table of Claim 9, further comprising a second inverter having an input terminal coupled to the LUT output terminal.

11. (Original) A configurable logic block (CLB) in a field programmable gate array (FPGA), the CLB comprising:

a plurality of function generator input terminals;

a function generator output terminal;

a registered output terminal;

a lookup table (LUT) comprising a plurality of LUT input terminals coupled to the plurality of function generator input terminals and a LUT output terminal coupled to the function generator output terminal; and

a register comprising a data input terminal programmably coupled to the output terminal of the LUT and a data output terminal coupled to the registered output terminal,

wherein the lookup table further comprises:

a plurality of configuration memory cells, each memory cell having an output terminal; and

a plurality of CMOS pass gates coupled between the output terminal of each memory cell and the LUT output terminal, wherein each path between one of the memory cells and the LUT output terminal traverses at least two of the CMOS pass gates, the two CMOS pass gates being coupled to two different ones of the LUT input terminals.

12. (Original) The CLB of Claim 11, wherein each path between one of the memory cells and the LUT output terminal traverses four of the CMOS pass gates.

13. (Original) The CLB of Claim 12, wherein the four CMOS pass gates traversed by each path are coupled to four different ones of the LUT input terminals.

14. (Original) The CLB of Claim 12, wherein the plurality of memory cells comprises 16 memory cells.

15. (Original) The CLB of Claim 11, the plurality of CMOS pass gates including an additional CMOS pass gate on the path between each memory cell and the LUT output terminal, the lookup table further comprising:

a plurality of additional LUT input terminals; and

a decoder circuit having input terminals coupled to the additional LUT input terminals and output terminals coupled to gate terminals of the additional CMOS pass gates.

16. (Original) The CLB of Claim 15, wherein the plurality of LUT input terminals comprises two input terminals and the plurality of additional LUT input terminals comprises two input terminals.

17. (Original) The CLB of Claim 16, wherein the plurality of memory cells comprises 16 memory cells.

18. (Original) The CLB of Claim 15, wherein the decoder circuit comprises:

a plurality of inverters having input terminals coupled to the plurality of additional LUT input terminals and further having output terminals; and

a plurality of NAND gates having input terminals coupled to the plurality of additional LUT input terminals and to the output terminals of the plurality of inverters and further having output terminals coupled to gate terminals of the additional CMOS pass gates.

19. (Original) The CLB of Claim 11, wherein the lookup table further comprises a first inverter having an input terminal coupled to the LUT output terminal and an output terminal coupled to the function generator output terminal of the CLB.

20. (Original) The CLB of Claim 19, wherein:

the CLB further comprises a carry logic circuit; and

the LUT further comprises a second inverter having an input terminal coupled to the LUT output terminal and an output terminal coupled to the carry logic circuit.